

**R09**

**Code No: D5803**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M.Tech II - Semester Examinations, March/April 2011**

**ADVANCED COMPUTER ARCHITECTURE  
(COMPUTER SCIENCE AND ENGINEERING)**

**Time: 3hours**

**Max. Marks: 60**

**Answer any five questions  
All questions carry equal marks**

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1. a) Define performance. Describe how the five levels of programs are used in evaluating performance.  
b) How Amdahl's law is useful for measurement of improved performance of computer systems? [6+6]
2. a) Explain various operations in the instruction set.  
b) Write notes on addressing modes for control flow instructions. [6+6]
3. a) What are the limitations of dynamically scheduled pipelines and how hardware based speculation can address these limitations?  
b) Briefly explain basic VLIW approach. [6+6]
4. a) Write short notes on RLSC.  
b) Give a brief account on Instruction-level parallelism. [6+6]
5. a) What is meant by dynamic scheduling? Explain.  
b) Explain the cost and performance of a cluster for transaction processing. [6+6]
6. Explain multiprocessor cache coherence. [12]
7. Explain Designing of clusters with example. [12]
8. Write short notes on the following:  
a) Practical issues in interconnecting networks.  
b) Protection of virtual memory. [6+6]

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FIRSTRANKER